

Sri Venkateswara University, Tirupati

Model Syllabus for 4-Year UG Honours in B.Sc. (Electronics) as Major in
consonance with Curriculum framework w.e.f. AY 2025-26

COURSE STRUCTURE (for Semester I to VI)

Year	Semester	Course	Title of the Course	No. of Hrs /Week	No. of Credits
I	I	1	Fundamental of Electricity and Electronics	3	3
			Fundamental of Electricity and Electronics Practical Course	2	1
		2	Circuit theory and Electronic Devices	3	3
			Circuit theory and Electronic Devices Practical Course	2	1
	II	3	Semiconductor Devices and Materials	3	3
			Semiconductor Devices and Materials Practical Course	2	1
		4	Digital Electronics	3	3
			Digital Electronics Practical Course	2	1
II	III	5	Analog Circuits and Communication	3	3
			Analog Circuits and Communication Practical Course	2	1
		6	Microprocessor System	3	3
			Microprocessor System Practical Course	2	1
		7	Electrical and Electronics Instrumentation	3	3
			Electrical and Electronics Instrumentation Practical Course	2	1
	IV	8	Electronic Communication System	3	3
			Electronic Communication System Practical Course	2	1
		9	Microcontroller and Interfacing	3	3
			Microcontroller and Interfacing Practical Course	2	1
		10	Computer Network	3	3

Year	Semester	Course	Title of the Course	No. of Hrs /Week	No. of Credits
			Computer Network Practical Course	2	1
III	V	11	Cellular Mobile Communication	3	3
			Cellular Mobile Communication Practical Course	2	1
		12 A	Industrial Electronics	3	3
			Industrial Electronics Practical Course	2	1
		OR			
		12 B	Embedded System Design	3	3
			Embedded System Design Practical Course	2	1
		13 A	Digital System Design	3	3
			Digital System Design Practical Course	2	1
		OR			
		13 B	Consumer Electronics	3	3
			Consumer Electronics Practical Course	2	1
	VI	14 A	Power Electronics	3	3
			Power Electronics Practical Course	2	1
		OR			
		14 B	VLSI Design	3	3
			VLSI Design Practical Course	2	1
		15 A	Principles and Utility of Electronic Domestic Applications	3	3
			Principles and Utility of Electronic Domestic Applications Practical Course	2	1
		OR			
		15 B	Digital Signal Processing	3	3
			Digital Signal Processing Practical Course	2	1

Note: In the III Year (during the V and VI Semesters), students are required to select a pair of electives from one of the Two specified domains. For example: if set 'A' is chosen, courses 12 to 15 to be chosen as 12 A, 13 A, 14 A and 15 A or if set 'B' is chosen, It is to be chosen as 12 B, 13 B, 14 B and 15 B to ensure in-depth understanding and skill development in the chosen domain, students must continue with the same domain electives in both the V and VI Semesters.

T. Ashuraman

SEMESTER - II

COURSE 4: DIGITAL ELECTRONICS

Theory

Credits: 3

3 hrs/week

Course Objectives :

To understand the number systems, Binary codes and Complements.

1. To understand the Boolean algebra and simplification of Boolean expressions.
2. To analyze logic processes and implement logical operations using combinational logic circuits.
3. To understand the concepts of sequential circuits and to analyze sequential systems in terms of state machines.
4. To understand characteristics of memory and their classification.
5. To implement combinational and sequential circuits using VHDL.

Unit – I (9 Hrs)

NUMBER SYSTEM AND CODES: Decimal, Binary, Hexadecimal, Octal. Codes: BCD, Gray and Excess-3 codes- code conversions- Complements (1's, 2's, 9's and 10's), Addition -Subtraction using complement methods.

Unit- II (9 Hrs)

BOOLEAN ALGEBRA AND THEOREMS: Boolean Theorems, De-Morgan's laws. Digital logic gates, Multi level NAND & NOR gates. Standard representation of logic functions (SOP and POS), Minimization Techniques (Karnaugh Map Method: 2,3 variables).

Unit-III (9 Hrs)

COMBINATIONAL DIGITAL CIRCUITS:

Adders-Half & full adder, Subtractor-Half and full subtractors, Parallel binary adder, Magnitude Comparator, Multiplexers (4:1) and Demultiplexers (1:4), Encoder (8- line-to-3- line) and Decoder (3-line-to-8-line). IC-LOGIC FAMILIES: TTL logic, CMOS Logic families(NAND&NOR Gates).

UNIT-IV (9 Hrs)

SEQUENTIAL DIGITAL CIRCUITS:

Flip Flops: S-R FF , J-K FF, T and D type FFs, Master-Slave FFs, Excitation tables, Registers:- Serial In Serial Out and Parallel In and Parallel Out, Counters Asynchronous- ,Mod-8,Mod- 10,Synchronous-4-bit &Ring counter.

UNIT- V (9 Hrs)

MEMORY DEVICES:

General Memory Operations, ROM, RAM (Static and Dynamic), PROM, EPROM, EEPROM, EAROM,

TEXT BOOKS:

1. M. Morris Mano, "Digital Design" 3rd Edition, PHI, New Delhi.
2. Ronald J. Tocci, "Digital Systems-Principles and Applications" 6/e. PHI, New Delhi. 1999. (UNITS I to IV)
3. G.K. Kharate-Digital electronics-oxford university press
4. S. Salivahana & S. Arivazhagan-Digital circuits and design
5. Fundamentals of Digital Circuits by Anand Kumar

Reference Books :

1. Herbert Taub and Donald Schilling, "Digital Integrated Electronics", McGraw Hill. 1985.
2. S.K. Bose, "Digital Systems". 2/e. New Age International. 1992.
3. D.K. Anvekar and B.S. Sonade, "Electronic Data Converters: Fundamentals & Applications". TMH. 1994.
4. Malvino and Leach, "Digital Principles and Applications". TMG Hill Edition.

SEMESTER - II

COURSE 4: DIGITAL ELECTRONICS

Practical

Credits: 1

2 hrs/week

Course Outcomes:

1. Develop a digital logic and apply it to solve real life problems.
2. Analyze, design and implement combinational logic circuits.
3. Classify different semiconductor memories.
4. Analyze, design and implement sequential logic circuits.
5. Simulate and implement combinational and sequential logic circuits using VHDL

List of Experiments:

1. Verification of IC-logic gates
2. Realization of basic gates using discrete components (resistor, diodes & transistor)
3. Realization of basic gates using Universal gates (NAND & NOR gates)
4. Verify Half adder and full adder using gates
5. Verify Half subtractor and full subtractor using gates.
6. Verify the truth table Multiplexer and demultiplexer.
7. Verify the truth table Encoder and decoder.
8. Verify the truth table of RS , JK, T-F/F using NAND gates
9. 4-bit binary parallel adder and subtractor using IC 7483
10. BCD to Seven Segment Decoder using IC -7447/7448

T. Raghuraman

**4- Year UG Honours, Major
Syllabus
(2025-26)
Semester-II**

Model Question Paper

Time : 3hrs

Marks:75

Part-A

Answer any Five Questions. Each Question carries 3 Marks.

5x3=15

- 1.
- 2.
- 3.
- 4.
- 5.
- 6.
- 7.
- 8.
- 9.
- 10.

Answer the following questions. Each question carries 12 Marks

5x12=60

11. a) Unit-I
(Or)
b) Unit-I

12. a) Unit-II
(Or)
b) Unit-II

13. a) Unit-III
(Or)
b) Unit-III

14. a) Unit-IV
(Or)
b) Unit-IV

15. a) Unit-V
(Or)
b) Unit-V